PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10065503	10/25/2002	714	726	2133	

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KERVEROS

**CONTINUING DATA VERIFIED: NONE

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** FOREIGN APPLICATIONS VERIFIED: NONE

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PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		BUR920010217US1
Verified and Acknowledged Examiners's intials			

TITLE : Testing logic and embedded memory in parallel

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U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

X 733

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED: Total Claims	Print Claim for O.G
ISSUE FEE: Amount Due	Date Paid		DRAWING: Sheets Drwg.	Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAMER		Primary Examiner / PREPARED FOR ISSUE	Application Examiner	

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